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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/625,843	07/26/2000	Hiroki Hiyama	35.C14640	7974

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EXAMINER	
AGGARWAL, YOGESH K	
ART UNIT	**PAPER NUMBER**
2622	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/625,843	HIYAMA ET AL.	
	Examiner	Art Unit	
	Yogesh K. Aggarwal	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14 and 16-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed 02/16/2007 have been fully considered but they are not persuasive.

Examiner's response:

2. Applicant argues with regards to claim 14 that in Nakamura as shown in figure 4, a charge is transferred once as shown in Fig. 4B, and a different charge is transferred as shown in Fig. 4D and according to the present invention, as is apparent from Fig. 1 C, the charge transferred in the second transfer is a remainder of the same charge which was transferred in the first transfer. The Examiner respectfully disagrees. Nakamura teaches in figure 4a charge Q1 being accumulated. In figures 4b and 4c, a part of the charge Q1 is transferred by resetting and transferring the reset transistor 34 and transfer transistor 32 on respectively and other part Q2 is left in the detection node 33 (col. 6 lines 34-65). In figure 4d, the photodiode accumulates charge Q3. In figures 4e and 4f, charges Q2 and Q3 are added and then read out (col. 6 line 66-col. 7 line 24, figure 5 and 6). Therefore charges are transferred by transferring a part of the signal charge (Q 1) and the other part (Q2), which was left from Q1 to the floating diffusion detection node 33. Therefore part of the charge Q1 is transferred and other part Q2 of the same charge is being transferred next along with newly added charge Q3.

3. Applicant argues with regards to claim 14 that no reset of diffusion region takes place in between the two transfer steps. However Nakamura teaches in col. 8 lines 21-41 figure 8, applying a plurality pulses to the transfer switch 22 to transfer the signal charge completely so that no image lags or linearity problems will arise to the floating diffusion unit 26. A pulse phi (addr) follows in order to transfer the signal charge to the vertical line 28, See col. 5 line 64-col.

6 line 2. Therefore combining the embodiments of figure 4 and figure 8 of Nakamura, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have used transferred charges Q1 and Q3 without resetting as taught in col. 8 lines 21-41 figure 8 when used in figure 4 of Nakamura in order to have no image lag thereby having an image which is better in quality when reproduced on a display device.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 14, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (US Patent # 6,930,722) in view of Hiyama et al. (US Patent # 6,963,372).

[Claims 14 and 18]

Nakamura teaches a driving method for a MOS type image pickup device having pixels each including a photoelectric conversion unit (figure 2 pixel 21), a transfer MOS transistor (22) for transferring a photoelectric conversion signal charges generated by said photoelectric conversion unit (21) to a floating diffusion unit (detection node 26) at an input terminal of an amplifier element (amplification transistor 23 inherently has a forward diffusion e.g. detection node present at an input terminal), wherein the image pickup device includes signal lines (28) outputting the amplified signal to a line memory (figure 1, line memory 12) arranged at each signal line (col. 5 lines 24-col. 6 line 2), comprising

a driving step comprising a first step and second step, said first step being performed for applying a pulse to the transfer switch to transfer a part of the signal charges generated by said photoelectric conversion unit to the floating diffusion region, and said second transfer step being performed subsequently to said first transfer step, for applying a pulse to the transfer switch to transfer the other part of the signal charges generated by said photoelectric conversion unit to the floating diffusion, before reading out a signal from the pixel to the signal line (in figure 4a charge Q1 being accumulated. In figures 4b and 4c, a part of the charge Q1 is transferred by resetting and transferring the reset transistor 34 and transfer transistor 32 on respectively and other part Q2 is left in the detection node 33 (col. 6 lines 34-65). In figure 4d, the photodiode accumulates charge Q3. In figures 4e and 4f, charges Q2 and Q3 are added and then read out (col. 6 line 66-col. 7 line 24, figure 5 and 6). Therefore charges are transferred by transferring a part of the signal charge (Q1) and the other part (Q2) to the floating diffusion 33).

Nakamura fails to teach no reset of diffusion region takes place in between the two transfer steps and no effective quantity of light is incident on the photoelectric device. However Nakamura teaches in col. 8 lines 21-41 figure 8, applying a plurality pulses to the transfer switch 22 to transfer the signal charge completely so that no image lags or linearity problems will arise to the floating diffusion unit 26. A pulse phi (addr) follows in order to transfer the signal charge to the vertical line 28, See col. 5 line 64-col. 6 line 2. Since the dark signals are read after the light accumulated signals are readout there is no effective quantity of light incident on the photoelectric device . Therefore combining the embodiments of figure 4 and figure 8 of Nakamura, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have used transferred charges Q1 and Q3 without resetting and no effective quantity

of light incident on the photoelectric device as taught in col. 8 lines 21-41 figure 8 when used in figure 4 of Nakamura in order to have no image lag thereby having an image which is better in quality when reproduced on a display device.

Nakamura teaches a line memory 12 (figure 1) and a MOS type image pick up device but fails to disclose a CMOS image pick up device that outputs the charges to a capacitor on a signal line and a switch element for controlling electric continuity of the signal line and the capacitor.

However Hiyama teaches a CMOS image pickup device includes signal lines (V1 and V2 as shown in figure 13) outputting the amplified signal to a capacitor (CTN and CTS, figure 13) arranged at each signal line and a switch element (M5) for controlling electric continuity of the signal line and the capacitor (col. 14 lines 58-66, col. 15 lines 4-17, col. 5 lines 45-59).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention have a CMOS image pick up device that outputs the charges to a capacitor on a signal line and a switch element for controlling electric continuity of the signal line and the capacitor to be used in the system of Nakamura as a line memory in order to store the signal and reset and thereby to use the signal and reset to remove the fixed pattern noise in a CDS operation.

[Claims 16 and 17]

Hiyama teaches a phi. RES pulse (figure 15) being applied to a reset transistor (M1), then the gate of the pixel amplifier M3 is reset. A signal phi. TX1 becomes high at time t75, and photo-charge is transferred to the gate of pixel amplifier (col. 17 lines 1-17) and thereafter the phi. SEL1 and phi. TS are changed to high at time t78 and photocharges are read out. The differential block 73 takes the difference between V1S to VnN and the corresponding noise signals V1N to

VnN, and sequentially outputs the differences as a voltage VOUT (col. 17 lines 35-47). This process is commonly known as CDS and the signals are called correlated signals.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571)-272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

YKA
October 27, 2007

LIN YE
SUPERVISORY PATENT EXAMINER